IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Chia-Lin Chen, et al.	§	Docket No.:	24061.42
Serial No.:	10/712,460	§	Examiner:	To Be Determined
Filed:	November 13, 2003	§	Art Unit:	1746
Entitled:	SEMICONDUCTOR WAFER MANUFACTURING METHODS EMPLOYING CLEANING DELAY PERIOD	§	Conf. No.:	9316

INFORMATION DISCLOSURE STATEMENT

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty of disclosure under 37 CFR §1.56, and in accordance with the practice under 37 CFR §1.97 and §1.98, the Examiner's attention is directed to the documents listed on the enclosed modified Form PTO-1449. No inference should be made that the cited references are in fact material, are in fact prior art, or that no better art exists. The cited patents are listed in numerical and alphabetical order and are not listed in any order based on their pertinence.

The above-identified application was filed after June 30, 2003. Therefore, pursuant to the waiver of the requirement under 37 CFR 1.98 (a)(2)(i) as stated in a Pre-OG Notice dated July 11, 2003, copies of the U.S. patents listed on the enclosed modified Form PTO-1449 are not being provided.

This Information Disclosure Statement is being filed within three months of the United States filing date or before the mailing date of a first Office Action on the merits. No certification or fee is required (37 CFR §1.97(b)).

The Commissioner is hereby authorized to charge any additional fees which may be required or credit any overpayment to Deposit Account 08-1394.

It is respectfully requested that the above information be considered by the Examiner and that a copy of the enclosed Form PTO-1449 be returned indicating that such information has been considered.

Respectfully submitted,

Timothy F. Bliss
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Date: 4/12/04

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Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

Gayle Conner
Name

4-12-04
Date

In place of PTO-1449 Form	U. S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	10/712,460
				Filing Date	November 13, 2003
				Applicant(s)	Chia-Lin Chen, et al.
				Art Unit	1746
				Examiner Name	To Be Determined
SHEET	1	OF	1	Attorney Docket Number	24061.42 (TSMC2002-1015)

U. S. PATENT DOCUMENTS				
Examiner's Initials	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
	AA	2002/0009900	01/24/02	Tay et al.
	AB	5,371,396	12/06/94	Vinal et al.
	AC	5,521,127	05/28/96	Hori et al.
	AD	5,710,450	01/20/98	Chau et al.
	AE	5,840,125	11/24/98	Gronet et al.
	AF	5,943,230	08/24/99	Rinnen et al.
	AG	5,959,333	09/28/99	Gardner et al.
	AH	6,020,260	02/01/00	Gardner
	AI	6,099,647	08/08/00	Yich et al.
	AJ	6,110,812	08/28/00	Ho et al.
	AK	6,114,258	09/05/00	Miner et al.
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	AM	6,207,304	03/27/01	Law et al.
	AN	6,242,776	06/05/01	Hause et al.
	AO	6,323,094	11/27/01	Wu
	AP	6,326,664	12/04/01	Chau et al.
	AQ	6,399,445	06/04/02	Hattangady, et al.
	AR	6,402,850	06/11/02	Beinglass et al.
	AS	6,410,090	06/25/02	Wang
	AT	6,413,871	07/02/02	M'Saad et al.
	AU	6,450,116	09/17/02	Noble et al.
	AV	6,482,726	11/19/02	Aminpur et al.
	AW	6,488,776	12/03/02	Wang
	AX	6,518,203	02/11/03	Narwankar et al.

FOREIGN PATENT DOCUMENTS					
Examiner's Initials	Cite No.	Foreign Patent Document (Country Code – Number – Kind)	Publication Date MM-DD-YYYY	Patentee or Applicant of Cited Document	Translation Y/N

OTHER PRIOR ART		
Examiner's Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item, date, page(s), volume-issue number(s), publisher, city/country where published
	AY	ARNUAD, F., ET AL., "Gate Oxide Process Impact on RNCE for Advanced CMOS Transistors", September 2002, ESSDERC '02, Firenze Italy, 21 pages.
	AZ	LI, GENE, "Total Solutions for Front-End Thermal Processing", Foresight, May 2001, Pages 41-45.
	BA	ZONCA, R., ET AL., "Ultra Thin NO/N_2O Oxynitride Dielectric for Advanced Flash Memory Application: Single Wafer and Batch Technology", 6 pages.
	BB	"Gate Stack", World Wide Web http://www.appliedmaterials.com/products/gate_stack.html, printed on February 17, 2003, 1 page.
	BC	"Technology Challenges for 100nn and Beyond Transistor and Capacitor Fabrication: Fig. 8", World Wide Web http://www.future-fab.com/assets/images/FFI11E1104F8.htm, printed on February 18, 2003, 1 page.

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.